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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	4181US (96-973.2)
First Inventor or Application Identifier	Salman Akram
Title	See 1 in Addendum
Express Mail Label No.	EL700255248US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

1. [X] * Fee Transmittal Form *(e.g., PTO/SB/17)* *(Submit an original, and a duplicate for fee processing)*
2. [X] Specification [Total Pages 47] *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 U.S.C. 113)* [Total Sheets 6]
4. Oath or Declaration [Total Pages 2]
   a. [X] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 C.F.R. § 1.63(d)) *(for continuation/divisional with Box 17 completed)* ***[Note Box 5 below]***
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).
5. [X] Incorporation By Reference *(useable if Box 4b is checked)* The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet & document(s))
9. [ ] 37 C.F.R.§3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [X] Information Disclosure Statement (IDS)/PTO-1449 [X] Copies of IDS Citations
12. [ ] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
14. [ ] * Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application, Status still proper and desired
15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [ ] Other. .....

* *A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon.*

17. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in a preliminary amendment:*

[ ] Continuation [ ] Divisional [X] Continuation-in-part (CIP) of prior application No: 09/292,655

Prior application information: Examiner Unknown Group / Art Unit: 2786

18. CORRESPONDENCE ADDRESS

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Addendum

1. METHOD FOR USING DATA REGARDING MANUFACTURING PROCEDURES INTEGRATED CIRCUITS (IC'S) HAVE UNDERGONE, SUCH AS REPAIRS, TO SELECT PROCEDURES THE IC'S WITH UNDERGO, SUCH AS ADDITIONAL REPAIRS

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APPLICATION FOR LETTERS PATENT

for

METHOD FOR USING DATA REGARDING MANUFACTURING PROCEDURES INTEGRATED CIRCUITS (IC'S) HAVE UNDERGONE, SUCH AS REPAIRS, TO SELECT PROCEDURES THE IC'S WILL UNDERGO, SUCH AS ADDITIONAL REPAIRS

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METHOD FOR USING DATA REGARDING MANUFACTURING PROCEDURES INTEGRATED CIRCUITS (IC'S) HAVE UNDERGONE, SUCH AS REPAIRS, TO SELECT PROCEDURES THE IC'S WILL UNDERGO, SUCH AS ADDITIONAL REPAIRS

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation-in-part of application Serial No. 09/292,655, filed April 15, 1999, pending which is a continuation of application Serial No. 08/871,015, filed June 6, 1997, pending, which is related to: a co-pending application having Serial No. 08/591,238, filed January 17, 1996, entitled "METHOD AND APPARATUS [sic] FOR STORAGE OF TEST RESULTS WITHIN AN INTEGRATED CIRCUIT", abandoned in favor of a continuation-in-part application filed February 27, 1998, having Serial No. 09/032,417, and entitled "METHOD AND APPARATUS [sic] FOR STORAGE OF TEST RESULTS WITHIN AN INTEGRATED CIRCUIT"; a co-pending application having Serial No. 08/664,109, filed June 13, 1996, entitled "A STRUCTURE AND A METHOD FOR STORING INFORMATION IN A SEMICONDUCTOR DEVICE", now pending; a co-pending application filed January 17, 1997 having Serial No. 08/785,353 and entitled "METHOD FOR SORTING INTEGRATED CIRCUIT DEVICES", now pending; a co-pending application filed February 17, 1997 having Serial No. 08/801,565 and entitled "METHOD OF SORTING A GROUP OF INTEGRATED CIRCUIT DEVICES FOR THOSE DEVICES REQUIRING SPECIAL TESTING", allowed; a co-pending application filed February 26, 1997 having Serial No. 08/806,442 and entitled "METHOD IN AN INTEGRATED CIRCUIT (IC) MANUFACTURING PROCESS FOR IDENTIFYING AND RE-DIRECTING IC'S MIS-PROCESSED DURING THEIR MANUFACTURE", now pending; and a co-pending application filed March 24, 1997 having Serial No. 08/822,731 and entitled "METHOD FOR CONTINUOUS, NON LOT-BASED INTEGRATED CIRCUIT MANUFACTURING", now pending.

BACKGROUND OF THE INVENTION

Field of the Invention: The present invention relates in general to integrated circuit semiconductor device (IC) manufacturing. More specifically, it relates to methods in IC manufacturing processes for using data regarding manufacturing procedures IC's have undergone, such as repair procedures, to select procedures the IC's will undergo, such as additional repair procedures.

State of the Art: As shown in FIG. 1, a typical process 10 for manufacturing very small electronic semiconductor device circuits referred to as "Integrated Circuits" (IC's) begins with the IC's being formed or "fabricated" on the surface of a wafer 12 of semiconductor material, such as silicon. Once fabricated, IC's are electronically probed to determine whether they are functional (i.e., "good") or nonfunctional (i.e., "bad"). If any IC's are found to be bad, an attempt is made to repair those IC's by replacing nonfunctional circuit elements in the IC's with spare circuit elements. For example, Dynamic Random Access Memory (DRAM) IC's are typically repaired by replacing nonfunctional rows or columns of memory cells in the IC's with spare rows or columns.

These repairs are not always successful, because the number of spare circuit elements on an IC may be exhausted before all nonfunctional circuit elements on the IC are replaced, and because some circuit elements on IC's have no spares to replace them. As a result, a number of bad IC's typically remain on a wafer 12 even after attempts are made to repair the IC's. The location of bad IC's on a wafer 12, along with the location of any good IC's on the wafer 12, is typically stored in a computer database commonly referred to as a "wafer map."

After being probed and, if necessary, repaired, IC's begin an assembly process with their wafer 12 being mounted on an adhesive film. In some instances, the film is a special high-adhesion Ultraviolet (U.V.) film. Without cutting the adhesive film, IC's are sawed from their wafer 12 into discrete IC dice or "chips" using high-speed precision dicing equipment. IC dice mounted on U.V. film are then exposed to U.V. light to loosen the grip of the film on the dice. IC dice identified as good by their wafer map are then each "picked" by automated equipment from their sawed wafer 12 and its associated film and "placed" on an epoxy coated bonding site of one lead frame in a strip of

interconnected lead frames, while IC dice identified as bad are discarded into a scrap bin 14. The epoxy attaching the good IC dice to their lead frames is then cured, and the attached dice are wire bonded to their lead frames using high speed bonding equipment.

Once wire bonded, IC dice and their associated lead frames are formed into IC packages using a hot thermosetting plastic encapsulant injected into a mold. IC packages are then cured to set their plastic encapsulant. After encapsulation and curing, leads of the lead frames projecting from the packages are dipped in a cleansing chemical bath in a process referred to as "de-flash" and then electroplated with a lead/tin finish. Connections between lead frames in lead frame strips are then cut to "singulate" IC packages into discrete IC devices.

After assembly, discrete IC devices are tested in a simple electronic test referred to as an "opens/shorts" test, which checks for "opens" (i.e., no connection) within the devices where connections should exist and "shorts" (i.e., a connection) where connections should not exist. Devices that pass the opens/shorts test proceed on through the process 10 to various burn-in and test procedures where they are tested for functionality, operability, and reliability, and devices that pass these burn-in and test procedures are then typically shipped to customers.

IC devices that fail any of the opens/shorts, burn-in, and test procedures are checked to determine whether they are repairable. This "check" typically includes an electronic "querying" of a device to determine whether enough spare circuit elements remain in the device to effect necessary repairs. Devices determined to be unrepairable are scrapped in a scrap bin 16, while devices that are repairable are repaired, typically by replacing nonfunctional circuit elements in the devices with spare circuit elements in the same manner as described above. After being repaired, these devices then reenter the manufacturing process 10 just prior to the opens/shorts, burn-in, or test procedures they failed.

Electronic querying of IC devices to determine whether spare circuit elements are available to effect repairs increases the time required to move the devices through the manufacturing process 10 and places an additional burden on expensive testing resources. While the extra time added by querying one IC device may be insignificant, the time

required to query thousands and thousands of IC devices adds up and can result in a significant reduction in the number of IC devices completing the manufacturing process 10 in a given amount of time. Therefore, there is a need in the art for a method of determining whether enough spare circuit elements are available in an IC device to effect repairs without having to query the device.

Similarly, as shown in FIG. 2, a typical process 20 for manufacturing so-called "flip-chip" and "Chip-On-Board" (COB) Multi-Chip Modules (MCM's), in which multiple IC dice are typically attached directly to a substrate, such as a printed circuit board (PCB), begins with IC's being fabricated on the surface of a semiconductor wafer 22 in the same manner as described above. Once fabricated, IC's are electronically probed to determine whether they are good or bad, and if any IC's are found to be bad, an attempt is made to repair those IC's (i.e., make them good IC's) by replacing nonfunctional circuit elements in the IC's with spare circuit elements. The locations of good and bad IC's on a wafer 22 are then typically stored in an electronic wafer map.

After being probed and, if necessary, repaired, IC's begin an assembly process with their wafer 22 being mounted on an adhesive film. Without cutting this film, IC's are then sawed from their wafer 22 into discrete IC dice using high-speed precision dicing equipment. IC dice that are mounted on the special high-adhesion U.V. film described above are then exposed to U.V. light to loosen the grip of the film on the dice.

IC dice identified as good by their electronic wafer map are then each picked by automated equipment from their sawed wafer 22 and its associated film, typically for attachment to a substrate in a panel of multiple substrates, such as a panel of interconnected PCB's. If the assembly process is a flip-chip process, picked dice are then flipped and directly attached at their active, frontside surfaces to substrates to form MCM's. If the assembly process is a COB process, picked dice are directly attached at their inactive, backside surfaces to adhesive coated bonding sites of substrates to form MCM's. IC dice identified as bad are discarded into a scrap bin 24.

Panels of MCM's are then cured. If the assembly process is a COB process, the MCM's may be plasma cleaned, if necessary, and the COB IC dice are then wire bonded to their substrates using high speed bonding equipment.

After assembly, panels of MCM's are tested in an opens/shorts test. Panels having COB IC dice that pass the opens/shorts test proceed on through the manufacturing process 20 so the dice can be encapsulated using an overmold, hard cover, or so-called "glob" top, while panels having flip-chip IC dice that pass the opens/shorts test may have their dice encapsulated using an underfill followed by an overmold, hard cover, or glob top. As will be described in more detail below, alternatively flip-chip IC dice may be encapsulated after burn-in and test procedures. The disposition of panels of MCM's having COB and flip-chip attached IC dice that fail the opens/shorts test will be described in more detail below.

Panels of MCM's having both COB and flip-chip IC dice, including those panels having flip-chip IC dice that were not encapsulated, are then singulated into discrete MCM's, typically by a shear press or router. After singulation, those MCM's having encapsulated IC dice have their dice tested again in an additional opens/shorts test to check for problems caused by the encapsulation. MCM's having encapsulated dice that pass this additional opens/shorts test, as well as MCM's having dice that were not encapsulated, then proceed on in the manufacturing process 20 to various burn-in and test procedures. The disposition of any MCM's having encapsulated dice that fail the additional opens/shorts test will be described in more detail below.

After the burn-in and test procedures, MCM's having unencapsulated flip-chip IC dice that pass the procedures proceed on in the process 20 so their dice may be covered with an overmold, hardcover, or glob top. Dice covered in this manner are then checked in a further opens/shorts test for problems caused by their being covered, and MCM's having dice that pass this further test are then typically shipped to customers. MCM's having encapsulated IC dice that pass the burn-in and test procedures skip this final opens/shorts test and typically proceed to shipping.

MCM's having attached IC dice that fail any of the opens/shorts, burn-in, and test procedures are checked to determine whether their associated IC dice are repairable. This "check" typically includes an electronic querying of the IC dice to determine whether enough spare circuit elements remain in the dice for effecting repairs. MCM's determined to have unrepairable IC dice are then either reworked using replacement IC

dice in an expensive and time-consuming procedure or scrapped in a scrap bin 26, while MCM's having IC dice that are repairable are repaired, typically by replacing nonfunctional circuit elements in the IC dice with spare circuit elements. After being repaired, these MCM's then reenter the manufacturing process 20 just prior to the opens/shorts, burn-in, or test procedures they failed.

As discussed above, electronic querying of IC dice to determine whether spare circuit elements are available to effect repairs increases the time required to move MCM's through the manufacturing process 20 and places an additional burden on expensive testing resources. Also, IC dice that require repair, and are found to be unrepairable only after the assembly process, waste assembly time, materials, and resources and necessitate the scrapping or reworking of MCM's that may contain many functional dice. It is desirable, then, to have an IC manufacturing method for identifying unrepairable IC dice so they may be kept out of COB, flip-chip, and other MCM assembly processes.

As described in U.S. Patent No.'s 5,301,143, 5,294,812, and 5,103,166, some methods have been devised to electronically identify IC dice. Such methods take place "off" the manufacturing line, and involve the use of electrically retrievable identification (ID) codes, such as so-called "fuse ID's," programmed into individual IC dice to identify the dice. The programming of a fuse ID typically involves selectively blowing an arrangement of fuses or anti-fuses in an IC die using electric current or a laser so that when the fuses or anti-fuses are accessed, they output a preprogrammed ID code. Unfortunately, none of these methods addresses the problem of identifying unrepairable IC dice "on" a manufacturing line.

SUMMARY OF THE INVENTION

The present invention provides a method in an integrated circuit (IC) manufacturing process for using data regarding manufacturing procedures IC's have undergone, such as repair procedures at probe, to select manufacturing procedures the IC's will undergo, such as additional repair procedures during back-end testing. The IC's

are each programmed with a substantially unique identification (ID) code, such as a fuse ID.

The method includes storing data in association with the ID codes of the IC's that identifies manufacturing procedures the IC's have undergone. This data may identify spare circuitry already used to repair the IC's at probe, for example, or spare circuitry available to repair the IC's. The ID codes of the IC's are automatically read, for example, at an opens/shorts test during the manufacturing process. The data stored in association with the ID codes is then accessed, and manufacturing procedures the IC's will undergo, such as additional repair procedures during back-end testing, are selected in accordance with the accessed data. Thus, for example, the accessed data may indicate that insufficient spare circuitry is available on an IC to effect repairs, so the IC can proceed directly to a scrap bin without being "queried" to determine the availability of spare circuitry, as is traditionally necessary. The present invention thus eliminates the time-wasting conventional process of querying IC's prior to repair or scrapping.

Further embodiments include methods of manufacturing IC devices and Multi-Chip Modules (MCM's) which incorporate the method described above.

In an additional embodiment, a method in an MCM manufacturing process for diverting good but unrepairable IC dice from the process includes storing data in association with ID codes, such as fuse ID's, of the IC's that identifies IC's that are a) good and repairable, b) good but unrepairable, and c) bad. In the inventive method, the ID codes of the IC's are automatically read, and the data stored in association with the ID codes is accessed. IC's identified as good but unrepairable by the accessed data are diverted to other IC manufacturing processes, while IC's identified as bad are discarded, and IC's identified as good and repairable are assembled into MCM's.

The present invention thus prevents IC's that are unrepairable from being assembled into MCM's, such as Single In-Line Memory Modules (SIMM's), and thus prevents the reworking or scrapping of MCM's into which unrepairable IC's have been assembled.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

FIG. 1 is a flow diagram illustrating a conventional integrated circuit (IC) device manufacturing process;

FIG. 2 is a flow diagram illustrating a conventional Chip-On-Board (COB) or flip-chip attached IC manufacturing process;

FIG. 3A is a flow diagram illustrating an IC device manufacturing process in accordance with the present invention;

FIG. 3B is a flow diagram illustrating an assembly portion of the manufacturing process of FIG. 3A in more detail;

FIG. 4A is a flow diagram illustrating a COB or flip-chip multi-chip module IC manufacturing process in accordance with the present invention; and

FIG. 4B is a flow diagram illustrating an assembly portion of the manufacturing process of FIG. 4A in more detail.

DETAILED DESCRIPTION OF THE INVENTION

As shown in FIG. 3A, an inventive process 30 for manufacturing Dynamic Random Access Memory (DRAM) Integrated Circuit semiconductor devices (IC) devices begins with DRAM IC's being fabricated in a fabrication step 32 on the surface of a semiconductor wafer 34. It will be understood by those having skill in the field of this invention that the present invention is applicable to any IC devices, including Static Random Access Memory (SRAM) IC's, Synchronous DRAM (SDRAM) IC's, processor IC's, Single In-line Memory Modules (SIMM's), Dual In-line Memory Modules (DIMM's), Rambus In-Line Memory Modules (RIMM), Small Outline Rambus In-Line Memory Modules (SO-RIMM), Personal Computer Memory Format (PCMCIA), Board-Over-Chip type substrate configurations, and other Multi-Chip Modules (MCM's). It will also be understood that although the present invention will be described below in the context of a wire bond/lead frame assembly process, either a conventional lead frame or leads-over-chip configuration using adhesive tape on the lead frame or the semiconductor die or non-conductive adhesive on the active surface of the semiconductor die (LOC), the present invention is applicable to any IC assembly process, including, for example, Chip

On Board (COB) either single semiconductor device or the modular form of multiple semiconductor device IC's, Board Over Chip (BOC) either single semiconductor device or the modular form of multiple semiconductor device IC's, any configuration of substrate and component including Tessera style electrical components (film on elastomer), and flip-chip processes (as will be described below with respect to FIG.'s 4A and 4B), and Tape-Automated Bonding (TAB) processes, wafer scale semiconductor device packages or packaging, either the entire wafer as a whole, multiple semiconductor devices as portions of the wafer which are singulated and packaged, or the singulation of the semiconductor devices on the wafer which are later packaged and/or mounted.

Once fabricated, the DRAM IC's are electronically probed in a probe step 36 to determine whether they are good or bad, and if any DRAM IC's are found to be bad, an attempt is made to repair those IC's by replacing nonfunctional rows or columns in the IC's with spare rows or columns. The location of bad DRAM IC's on a wafer 34, along with the location of any good DRAM IC's on the wafer 34, is stored in a computer in an electronic wafer map in association with data identifying spare rows and columns still available in each of the DRAM IC's after any repairs performed at the probe step 36. Of course, it will be understood that the stored data may alternatively identify spare rows and columns used in each of the DRAM IC's to effect repairs at the probe step 36.

During the probe step 36, DRAM IC's fabricated on the wafers 34 are programmed in the manner described above with a fuse identification (ID) unique to each IC. The fuse ID for each DRAM IC is then stored in association with the repair data 38 for that IC. The fuse ID may identify, for example, a wafer lot ID, the week the DRAM IC's were fabricated, a wafer ID, a die location on the wafer, and a fabrication facility ID. As a result of storing the fuse ID for each DRAM IC in association with the repair data 38, the availability of spare rows or columns for effecting post-probe repairs in a particular DRAM IC can be determined by using the fuse ID of the IC to access the stored repair data 38 for the IC, as will be described in more detail below.

It will be understood, of course, that the present invention includes within its scope DRAM IC and other IC's having any ID code, such as a dot code, bar code, or any suitable type marking code on the IC's, including those having fuse ID's. It will also be

understood that the IC's may be programmed with their fuse ID's at steps in the manufacturing process 30 other than the probe step 36.

After being probed and, if necessary, repaired, DRAM IC's enter an assembly process 40 in which good IC's are assembled into IC devices, as will be described in more detail below with respect to FIG. 3B, while bad IC's are discarded in a scrap bin 42. In addition, DRAM IC's 44 that have been diverted from COB and flip-chip manufacturing process flows enter the assembly process 40 and are also assembled into IC devices. The DRAM IC's 44 are diverted from the COB and flip-chip process flows because so many of their spare rows and columns have been used at probe to effect repairs in the IC's 44 that the IC's 44 fall below a minimum threshold level of repairability, as will be described in more detail below with respect to FIG.'s 4A and 4B.

After the assembly process 40, discrete DRAM IC devices are tested in an opens/shorts test 46. There, the fuse ID of the DRAM IC in each IC device is automatically read and correlated with the repair data 38 produced in the manufacturing process 30 or repair data 48 produced in a COB or flip-chip process flow as described below. It should be understood that although the fuse ID's of DRAM IC's in the process 30 are typically read electronically, they may also be read optically if the fuse ID's consist of "blown" laser fuses that are optically accessible. It should also be understood that the fuse ID's of DRAM IC's may be read at steps in the process 30 other than the opens/shorts test 46.

DRAM IC devices that pass the opens/shorts test 46 proceed on through the process 30 to various burn-in and test procedures 50 and 52 where they are tested for functionality, operability, and reliability, and DRAM IC devices that pass these burn-in and test procedures 50 and 52 are shipped 54 to customers.

DRAM IC devices that fail any of the opens/shorts, burn-in, and test procedures 46, 50, and 52 proceed to repair 56. Those DRAM IC devices that do not have enough available spare rows and columns to effect repairs, and thus are unrepairable, are identified as such when their repair data 38 and 48 is accessed at the opens/shorts test 46, and these devices proceed directly to rework or a scrap bin 58 without the need to query them. Of course, DRAM IC devices that are identified by their repair data 38 and 48 as

being repairable are repaired, typically by replacing nonfunctional rows and columns with spare rows and columns in the same manner as described above. After being repaired, these DRAM IC devices then reenter the manufacturing process 30 just prior to the opens/shorts, burn-in, or test procedures 46, 50, and 52 they failed.

It should be understood, of course, that the present invention is applicable to situations in a wide variety of IC manufacturing processes in which data regarding manufacturing procedures the IC's have undergone, such as repair procedures at probe, may be accessed through the use of fuse ID's and other ID codes to determine procedures the IC's should undergo, such as post-probe repairs.

As stated above, the assembly process 40 of FIG. 3A is shown in more detail in FIG. 3B. In the process 40, probed and repaired semiconductor wafers enter a wafer saw step 60 and are mounted on an adhesive film. The film may be any one of a wide variety of adhesive films used for this purpose, including, for example, a special high-adhesion U.V. film. Without cutting the film, DRAM IC's are then sawed from their wafer into discrete IC dice using high-speed precision dicing equipment. DRAM IC dice that are mounted on the special high-adhesion U.V. film are then exposed to U.V. light in an optional U.V. exposure step 62 to loosen the grip of the film on the dice.

DRAM IC dice identified as good by their electronic wafer map are then each picked by automated equipment from their sawed wafer and its associated film in a die attach step 64 and placed on an epoxy coated bonding site of one lead frame in a strip of interconnected lead frames, while DRAM IC dice identified as bad are discarded into the scrap bin 42. In addition, DRAM IC dice 44 that have been diverted from COB and flip-chip manufacturing process flows enter the assembly process 40 and are also placed on an adhesive coated bonding site of one lead frame in a lead frame strip. These diverted DRAM IC's 44 will be described in more detail below with respect to FIG.'s 4A and 4B. The adhesive attaching the good DRAM IC dice to their lead frames is then cured, if required, in a cure step 66, and the attached dice are wire bonded to their lead frames using high speed bonding equipment in a wire bond step 68.

Once wire bonded, DRAM IC dice and their lead frames continue the assembly process 40 by being formed into DRAM IC packages using a hot thermosetting plastic

encapsulant injected into a mold in an overmold step 70. DRAM IC packages are then cured in a further cure step 72 to set their plastic encapsulant. After encapsulation and curing, leads of the lead frames projecting from the packages may be dipped in a cleansing chemical bath in a de-flash process 74 and then may be electroplated with a lead/tin finish if they are not already plated. Finally, connections between the lead frames of different DRAM IC packages are then cut in a singulate step 76 to separate the packages into discrete DRAM IC devices.

In another embodiment of the present invention shown in FIG. 4A, an inventive COB or flip-chip process 80 for manufacturing DRAM SIMM's begins with DRAM IC's being fabricated in a fabrication step 82 on the surface of a semiconductor wafer 84. It will be understood by those having skill in the field of this invention that the present invention is applicable to any IC devices, including SRAM IC's, SDRAM IC's, processor IC's, and modules using such IC devices, such as DIMM's, RIMM's, S0-RIMM's, PCMCIA's, COB's, BOC's, and other MCM's. It will also be understood that although the present invention will be described below in the context of both a COB and a flip-chip assembly process, the present invention is applicable to any IC assembly process, including, for example, Tape-Automated Bonding (TAB) processes, wafer scale processes including packaging, partial wafer scale processes including packaging, etc. It should be further understood that the present invention relates to any type IC that has been singulated by any type singulation process or apparatus, such as wafer saw singulation, laser apparatus singulation, laser/water apparatus singulation (cool laser singulation), water jet apparatus singulation, etc.

Once fabricated, the DRAM IC's are electronically probed in a probe step 86 to determine whether they are good or bad, and if any DRAM IC's are found to be bad, an attempt is made to repair the IC's by replacing nonfunctional rows or columns in the IC's with spare rows or columns. The locations of bad DRAM IC's on a wafer 84, along with the locations of any good DRAM IC's on the wafer 84, are stored in a computer in an electronic wafer map in association with data 48 identifying spare rows and columns still available in each of the DRAM IC's after any repairs performed at the probe step 86.

During the probe step 86, DRAM IC's fabricated on the wafers 84 are programmed in the manner described above with a fuse identification (ID) unique to each IC. The fuse ID for each DRAM IC is then stored in association with the repair data 48 for that IC. The fuse ID may identify, for example, a wafer lot ID, the week the DRAM IC's were fabricated, a wafer ID, a die location on the wafer, and a fabrication facility ID.

It will be understood, of course, that the present invention includes within its scope IC's having any ID code, including those having fuse ID's. It will also be understood that the IC's may be programmed with their fuse ID's at steps in the manufacturing process 80 other than the probe step 86.

After being probed and, if necessary, repaired, DRAM IC's enter an assembly process 90 in which good IC's are assembled into panels of physically interconnected DRAM SIMM's, as will be described in more detail below with respect to FIG. 4B, while bad IC's are discarded in a scrap bin 92. In addition, DRAM IC's 44 in which so many spare rows and columns have been used at the probe step 86 to effect repairs that the IC's 44 fall below a minimum threshold of repairability are diverted from the COB or flip-chip process 80 for use in the standard assembly process 40 of FIG.'s 3A and 3B. Although a "minimum threshold of repairability" can be set at any level, it might be set, for example, at a level at which statistically the available spare rows and columns in a DRAM IC would only be able to effect repairs in an unacceptably low percentage (e.g., 50%) of cases of failures. Thus, the diverted DRAM IC's 44 typically include those IC's that have exhausted their spare rows and columns in repairs at the probe step 86, and those IC's that have some, but not enough, spare rows and columns left after being repaired at the probe step 86.

The present invention thus prevents DRAM IC's that would be repairable in few or none of the possible cases of failure from being assembled into DRAM SIMM's and other MCM's, and thus prevents the waste of time and resources associated with scrapping or reworking MCM's into which such IC's have traditionally been assembled.

After the assembly process 90, panels of DRAM SIMM's are tested in an opens/shorts test 96. There, the fuse ID of each DRAM IC in each DRAM SIMM is

automatically read and correlated with the repair data 48. It should be understood that although the fuse ID's of DRAM IC's in the process 80 are typically read electronically, they may also be read optically if the fuse ID's consist of "blown" laser fuses that are optically accessible. It should also be understood that the fuse ID's of DRAM IC's may be read at steps in the process 80 other than the opens/shorts test 96.

When the manufacturing process 80 is a COB process, panels of DRAM SIMM's having COB IC dice that pass the opens/shorts test 96 proceed to an encapsulation step 98 so the dice can be encapsulated using an overmold, hard cover, or glob top. Alternatively, when the manufacturing process 80 is a flip-chip process, panels of DRAM SIMM's having flip-chip IC dice that pass the opens/shorts test 96 may have their dice encapsulated at the encapsulation step 98 using an underfill followed by an overmold, hard cover, or glob top. As will be described in more detail below, alternatively, the flip-chip IC dice may be encapsulated after burn-in and test procedures. The disposition of panels of DRAM SIMM's having IC dice that fail the opens/shorts test will be described in more detail below.

Panels of DRAM SIMM's having either COB or flip-chip IC dice, including those panels of SIMM's having flip-chip IC dice that were not encapsulated at the encapsulation step 98, are then singulated into discrete DRAM SIMM's at a singulation step 100 by, for example, a water jet or a shear press. This singulation step 100 may, for example, divide a "ten" panel of ten physically attached DRAM SIMM's into ten discrete DRAM SIMM's.

After singulation, DRAM SIMM's having encapsulated IC dice are tested again in an additional opens/shorts test 102 to check for problems caused by the encapsulation step 98. DRAM SIMM's having encapsulated dice that pass this additional opens/shorts test 102, as well as DRAM SIMM's having dice that were not encapsulated, then proceed on in the manufacturing process 80 to burn-in testing 104 and back-end testing 106. The disposition of those DRAM SIMM's having encapsulated IC dice that fail the additional opens/shorts test 102 will be described in more detail below. The fuse ID's of the IC dice in the DRAM SIMM's may also be automatically read at this additional opens/shorts test 102.

After the burn-in and test procedures 104 and 106, DRAM SIMM's having un-encapsulated flip-chip IC dice that pass the procedures 104 and 106 proceed on in the process 80 to an optional cover step 108 so their dice may be covered with an overmold, hardcover, or glob top. Dice covered in this manner are then checked in a further opens/shorts test 108 for problems caused by their being covered, and DRAM SIMM's having dice that pass this further test are then typically shipped in a shipping step 110 to customers. DRAM SIMM's having encapsulated IC dice that pass the burn-in and test procedures 104 and 106 skip this covering and final opens/shorts test step 108 and proceed to the shipping step 110. Of course, the fuse ID's of the IC dice in the DRAM SIMM's tested at any of the burn-in, back-end test, and opens/shorts test procedures 104, 106, and 108 may be automatically read at any one or all of those tests.

DRAM SIMM's having IC dice that fail any of the opens/shorts, burn-in, and test procedures 96, 102, 104, 106 and 108 proceed to repair 112. Those DRAM SIMM's having DRAM IC dice that do not have enough available spare rows and columns to effect repairs, and thus are unrepairable, are identified as such when their repair data 48 is accessed at any one of the opens/shorts, burn-in, and back-end tests 96, 102, 104, 106, and 108, and these SIMM's proceed directly to rework (described below) or a scrap bin 114 without the need to query them. Of course, DRAM SIMM's having DRAM IC dice identified by their repair data 48 as being repairable are repaired, typically by replacing nonfunctional rows and columns with spare rows and columns in the same manner as described above. After being repaired, these DRAM SIMM's then reenter the manufacturing process 80 just prior to the opens/shorts, burn-in, or test procedures 96, 102, 104, 106 or 108 they failed.

Those DRAM SIMM's that are reworkable by replacing one or more non-functioning IC dice proceed through a Known Good Die (KGD) process in which a DRAM KGD (*i.e.*, a burned-in, fully tested, fully functional DRAM) replaces the non-functioning IC dice on the SIMM's in a replacement step 116. The KGD repairs are then tested in a repair step 118, and if the repairs are successful, the repaired DRAM SIMM's reenter the manufacturing process 80 just prior to the back-end test procedures 106. If the

repairs are not successful, the DRAM SIMM's may return to the repair step 112 to be reworked again or, if they are not reworkable, to be scrapped in the scrap bin 114.

As stated above, the assembly process 90 of FIG. 4A is shown in more detail in FIG. 4B. In the process 90, probed and repaired semiconductor wafers enter a wafer saw step 120 and are mounted on an adhesive film. The film may be any one of a wide variety of adhesive films used for this purpose, including, for example, a special high-adhesion U.V. film. Without cutting the film, DRAM IC's are then sawed from their wafer into discrete DRAM IC dice using high-speed precision dicing equipment. DRAM IC dice that are mounted on the special high-adhesion U.V. film are then exposed to U.V. light in an optional U.V. exposure step 122 to loosen the grip of the film on the dice.

IC dice identified as good by their electronic wafer map are then each picked by automated equipment from their sawed wafer and its associated film at an attachment step 124. If the assembly process 90 is a flip-chip process, multiple picked dice are then flipped and directly attached at their active, frontside surfaces to a panel of PCB's or other substrates to form, for example, DRAM SIMM's. If the assembly process 90 is a COB process, multiple picked dice are directly attached at their inactive, backside surface to an adhesive coated bonding site of a panel of PCB's or other substrates to form, for example, DRAM SIMM's. DRAM IC dice identified as bad are discarded into the scrap bin 92, while DRAM IC dice 44 that have used so many of their spare rows and columns in repairs at the probe step 86 that they fall below the minimum threshold of repairability are diverted to the standard assembly process 40 of FIG.'s 3A and 3B. Panels of DRAM SIMM's are then cured at a cure step 126. If the assembly process 90 is a COB process, the panels may be plasma cleaned in an optional plasma cleaning step 128, if necessary, and the COB IC dice are then wire bonded at a wire bond step 130 to their DRAM SIMM's using high speed bonding equipment. DRAM SIMM's then proceed to the opens/shorts test 96 described above with respect to FIG. 4A.

Although the present invention has been described with reference to particular embodiments, the invention is not limited to these embodiments. For example, while the various steps of these embodiments have been described as occurring in a particular

order, it will be understood that these steps need not necessarily occur in the described order to fall within the scope of the present invention. Thus, the invention is limited only by the appended claims, which include within their scope all equivalent methods that operate according to the principles of the invention as described.

CLAIMS

What is claimed is:

1. An integrated circuit manufacturing process using data related to manufacturing procedures used previously that a plurality of integrated circuits of semiconductor devices have undergone for selecting manufacturing procedures a plurality of integrated circuits of a semiconductor devices are to undergo, each semiconductor device having integrated circuits and having a substantially unique identification code, the manufacturing process comprising:

storing data in association with the identification code of each semiconductor device identifying manufacturing procedures the semiconductor device has undergone;

automatically reading the identification code of each semiconductor device; and

accessing the data stored in association with the identification code of each semiconductor device.

2. The process of claim 1, further comprising:

selecting manufacturing procedures each semiconductor device undergoes in accordance with the accessed data.

3. The process of claim 1, wherein the step of storing data comprises storing data that identifies repairs performed semiconductor device.

4. The process of claim 3, wherein the semiconductor device comprises Dynamic Random Access Memory (DRAM) semiconductor device, wherein storing data comprises storing data that identifies spare rows and columns used in repairing the DRAM semiconductor device.

5. The process of claim 3, wherein the semiconductor device comprises Dynamic Random Access Memory (DRAM) semiconductor device, wherein storing data comprises storing data that identifies spare rows and columns available to effect repairs in the DRAM semiconductor device.

6. The process of claim 1, wherein the step of storing data comprises storing data at probe.

7. The process of claim 1, wherein the step of automatically reading the identification code of each semiconductor device comprises electrically retrieving a unique fuse ID programmed into each semiconductor device.

8. The process of claim 1, wherein the step of automatically reading the identification code of each semiconductor device comprises optically reading a unique ID code provided on each semiconductor device.

9. The process of claim 8, wherein the step of optically reading a unique identification code provided on each semiconductor device comprises optically reading a unique laser fuse ID programmed into each semiconductor device.

10. The process of claim 1, wherein the step of automatically reading the identification code of each semiconductor device comprises automatically reading the identification code of each semiconductor device at one of an opens/shorts test, a burn-in test, and a back-end test in the semiconductor device manufacturing process.

11. The process of claim 1, wherein the step of accessing the data stored in association with the identification code of each semiconductor device comprises accessing the data stored in association with the identification code of each semiconductor device at one of an opens/shorts test, a burn-in test, and a back-end test in the semiconductor device manufacturing process.

12. The process of claim 2, wherein selecting manufacturing procedures the semiconductor device undergoes in accordance with the accessed data comprises selecting repairs the semiconductor device undergoes in accordance with the accessed data.

13. The process of claim 12, wherein the semiconductor device comprises Dynamic Random Access Memory (DRAM) semiconductor device, wherein selecting repairs the semiconductor device undergoes comprises selecting spare rows and columns used to repair the DRAM semiconductor device.

14. The process of claim 2, wherein the step of selecting manufacturing procedures the semiconductor device undergoes in accordance with the accessed data comprises selecting whether the semiconductor device undergoes repair procedures.

15. The process of claim 14, wherein the semiconductor device comprise Dynamic Random Access Memory (DRAM) semiconductor device, wherein selecting whether the semiconductor device undergoes repair procedures comprises selecting whether the DRAM semiconductor device will be repaired in accordance with whether the accessed data indicates enough spare rows and columns are available in the semiconductor device to effect repairs.

16. The process of claim 2, wherein the step of selecting manufacturing procedures the semiconductor device will undergo in accordance with the accessed data comprises determining whether the semiconductor device will be assembled into Multi-Chip Modules (MCM's) in accordance with whether the accessed data indicates the semiconductor device is repairable.

17. The process of claim 1, further comprising assembling the semiconductor device into a packaged semiconductor device after the step of storing data and before the step of automatically reading the identification code of each semiconductor device.

18. A method of manufacturing integrated circuit semiconductor devices from semiconductor wafers, the method comprising:

providing a plurality of semiconductor wafers;

fabricating a plurality of semiconductor devices on each of the wafers;

causing each semiconductor device on each of the wafers to store a substantially unique identification code;

storing data in association with the identification code of each semiconductor device that identifies manufacturing procedures the semiconductor device has undergone;

separating each semiconductor device on each of the wafers from its wafer to form one semiconductor device of a plurality of semiconductor dice;

assembling each semiconductor device into a semiconductor device assembly;

automatically reading the identification code associated with each semiconductor device; and

accessing the data stored in association with the identification code associated with each semiconductor device.

19. The method of claim 18, further comprising:

selecting manufacturing procedures the semiconductor device undergoes in accordance with the accessed data.

20. The method of claim 18, wherein the step of fabricating a plurality of semiconductor devices on each of the wafers comprises fabricating semiconductor devices selected from a group comprising Dynamic Random Access Memory (DRAM) semiconductor device, Static Random Access Memory (SRAM) semiconductor devices, Synchronous DRAM (SDRAM) semiconductor devices, and processor semiconductor devices, Rambus in-line memory module type semiconductor devices, small outline Rambus in-line memory module type semiconductor devices, and personal computer memory format type semiconductor devices .

21. The method of claim 18, wherein the step of causing each semiconductor device on each of the wafers to store a substantially unique identification code comprises programming each semiconductor device on each of the wafers to permanently store a unique fuse ID.

22. The method of claim 18, wherein the step of programming each semiconductor device on each of the wafers to permanently store a unique fuse identification code comprises programming at least one of fuses and anti-fuses in each semiconductor device on each of the wafers to permanently store a unique fuse identification.

23. The method of claim 18, wherein the step of assembling each semiconductor device of the semiconductor dice into a semiconductor device assembly comprises:

picking each semiconductor device from its wafer;

placing each semiconductor device onto an epoxy coated bonding site of one lead frame of a plurality of lead frames;

curing the epoxy on the bonding site of each lead frame of the lead frames;

wire bonding each semiconductor device to its associated lead frame;

encapsulating each semiconductor device and its associated lead frame to form one of a plurality of semiconductor device assembly packages, each package having projecting leads;

curing each of the semiconductor device assembly packages;

de-flashing the projecting leads of each semiconductor device assembly package;

electroplating the projecting leads of each semiconductor device assembly package; and

singulating each semiconductor device assembly package into one semiconductor device assembly package of a plurality of discrete semiconductor device assembly packages.

24. The method of claim 18, wherein the step of assembling each semiconductor device into a semiconductor device assembly comprises assembling each semiconductor device into a semiconductor device assembly selected from a group comprising a wire bond/lead frame semiconductor device, a Chip-On-Board (COB) semiconductor device, a flip-chip semiconductor device, and a Board-Over-Chip (BOC) semiconductor device.

25. A method of manufacturing Multi-Chip Modules (MCM's) from semiconductor wafers, the method comprising:

providing a plurality of semiconductor wafers;

fabricating a plurality of semiconductor devices on each of the wafers;

causing each semiconductor device of the semiconductor devices on each of the wafers to store a substantially unique identification code;

storing data in association with the identification code of each semiconductor device of the semiconductor devices that identifies manufacturing procedures each semiconductor device of semiconductor devices has undergone;

separating each semiconductor device of the semiconductor devices on each wafer of the plurality of semiconductor wafers from its wafer to form one semiconductor device of a plurality of semiconductor devices;

assembling one or more of the semiconductor devices into each of a plurality of MCM's;

automatically reading the identification code of each semiconductor device of the semiconductor devices in each MCM of the plurality of MCM's; and

accessing the data stored in association with the identification code of each semiconductor device of the semiconductor devices in each MCM of the plurality of MCM's.

26. The method of claim 25, further comprising:

selecting manufacturing procedures the semiconductor devices will undergo in accordance with the accessed data.

27. The method of claim 25, wherein the MCM's are selected from a group comprising Single In-Line Memory Modules (SIMM's) and Dual In-line Memory Modules (DIMM's), Rambus In-Line Memory Modules (RIMM), Small Outline Rambus In-Line Memory Modules (SO-RIMM), Personal Computer Memory Format (PCMCIA), and Board-Over-Chip type substrate.

28. A method of manufacturing semiconductor devices from semiconductor wafers, the method comprising:

providing a plurality of semiconductor wafers;

fabricating a plurality of semiconductor devices on each of the wafers;

electronically probing each semiconductor device of the semiconductor devices on each wafer of the plurality of semiconductor wafers to identify good, bad and repairable semiconductor devices on each wafer of the plurality of semiconductor wafers;

repairing the repairable semiconductor devices;

programming each semiconductor device of the semiconductor devices on each wafer of the plurality of semiconductor wafers to store a unique fuse identification;

storing data in association with the fuse identification of each of the semiconductor devices identifying repairs performed on each semiconductor device of the semiconductor devices;

mounting each wafer of the plurality of semiconductor wafers on an adhesive film;

sawing each semiconductor device of the semiconductor devices on each wafer of the plurality of wafers from its wafer to form one of a plurality of discrete semiconductor devices;

automatically picking each semiconductor device of the semiconductor devices from its wafer;

placing each semiconductor device of the semiconductor devices onto an epoxy coated bonding site of one lead frame of a plurality of lead frames;

curing the epoxy on the bonding site of each lead frame of the lead frames;

wire bonding each semiconductor device of the semiconductor devices to its associated lead frame;

encapsulating each semiconductor device of the semiconductor devices and its associated lead frame to form one of a plurality of semiconductor device assembly packages each semiconductor device assembly package having projecting leads;

curing each semiconductor device assembly package;

de-flashing the projecting leads of each semiconductor device package;

electroplating the projecting leads of each semiconductor device package;

singulating each semiconductor device package;

testing each semiconductor device assembly package for opens and shorts;

burn-in testing each semiconductor device assembly package;

back-end testing each semiconductor device assembly package;

automatically reading the identification code of each semiconductor device assembly package;

accessing the data stored in association with the identification code of each semiconductor device assembly package;

for any semiconductor device assembly package failing any one of the opens/shorts, burn-in, and back-end tests, evaluating the accessed data to determine whether the failing semiconductor device assembly package may be repaired;

repairing any of the semiconductor device assembly package determined in accordance with the accessed data to be repairable and returning the repaired semiconductor device assembly package to the semiconductor manufacturing process; and

discarding any of the semiconductor device assembly package determined in accordance with the accessed data to be unrepairable.

29. The method of claim 28, wherein the step of mounting the wafers comprises mounting each wafer of the plurality of semiconductor wafers on an ultraviolet (U.V.) adhesive film, wherein the method further comprises exposing the U.V. adhesive film to U.V. light to loosen the wafers from the film prior to picking and placing the semiconductor device.

30. The method of claim 28, further comprising receiving a plurality of unrepairable semiconductor devices diverted from another semiconductor device manufacturing process.

31. A method of manufacturing Multi-Chip Modules (MCM's) from semiconductor wafers using Chip-On-Board (COB) techniques, the method comprising:

providing a plurality of semiconductor wafers;

fabricating a plurality of semiconductor devices on each wafer of the plurality of semiconductor wafers;

electronically probing each semiconductor device of the semiconductor devices on each wafer of the plurality of semiconductor wafers to identify good, bad and repairable semiconductor devices on each wafer of the plurality of semiconductor wafers;

repairing the repairable semiconductor devices;

programming each semiconductor device of the semiconductor devices on each wafer of the plurality of semiconductor wafers to store a unique fuse identification;

storing an electronic wafer map for each wafer that identifies the locations of good and bad semiconductor devices on the wafer and associates each unique fuse identification on the wafer with its fuse identification code;

storing data in association with the fuse identification code of each semiconductor device of the semiconductor devices identifying repairs performed on each semiconductor device of the semiconductor devices;

mounting each wafer of the plurality of semiconductor wafers on an adhesive film;

sawing each semiconductor device of the semiconductor devices on each wafer of the plurality of semiconductor wafers from its wafer to form one discrete semiconductor device;

accessing the stored wafer map for each wafer;

accessing the stored data for each semiconductor device on each wafer of the plurality of semiconductor wafers;

automatically picking each semiconductor device of the good semiconductor devices from its wafer;

discarding non-picked semiconductor devices identified as bad by the accessed wafer maps;

diverting picked semiconductor devices identified as good but unrepairable by the accessed wafer maps and data to a non-MCM semiconductor manufacturing process;

placing picked semiconductor devices identified as good and repairable by the accessed wafer maps and data onto epoxy coated bonding sites of a plurality of printed circuit boards using COB techniques to form a plurality of MCM's;

curing the epoxy on the bonding sites of each MCM of the plurality of MCM's;

wire bonding each of the semiconductor devices to its associated MCM;

testing each semiconductor device of the semiconductor devices on each MCM of the plurality of MCM's for opens and shorts;

encapsulating each semiconductor device of the semiconductor devices on each MCM of the plurality of MCM's;

retesting each semiconductor device of the semiconductor devices on each MCM of the plurality of MCM's for opens and shorts;

burn-in testing each semiconductor device of the semiconductor devices on each MCM of the plurality of MCM's;

back-end testing each semiconductor device of the semiconductor devices on each MCM of the plurality of MCM's;

automatically reading the fuse identification code of each semiconductor device in each MCM of the plurality of MCM's;

accessing the data stored in association with the fuse identification code of each semiconductor device of the semiconductor devices;

for any semiconductor device of the semiconductor devices failing any one of the opens/shorts, burn-in, and back-end tests, evaluating the accessed data to determine whether the failing semiconductor device may be repaired;

repairing any semiconductor device of the semiconductor devices determined in accordance with the accessed data to be repairable and returning the repaired MCM to the manufacturing process; and

replacing any semiconductor device of the semiconductor devices determined in accordance with the accessed data to be unrepairable with Known Good Die (KGD) dice and returning the repaired MCM to the manufacturing process.

32. The method of claim 31, further comprising plasma cleaning each MCM of the plurality of MCM's after curing the epoxy on the bonding sites of the MCM.

33. The method of claim 31, wherein the step of mounting the wafers comprises mounting each wafer of the plurality of semiconductor wafers on an Ultraviolet (U.V.) adhesive film, wherein the method further comprises exposing the U.V. adhesive film to U.V. light to loosen the wafer from the film prior to picking and placing the semiconductor device.

34. The method of claim 31, further comprising singulating the printed circuit boards associated with each MCM of the plurality of MCM's.

35. A method of manufacturing Multi-Chip Modules (MCM's) from semiconductor wafers using flip-chip techniques, the method comprising:

providing a plurality of semiconductor wafers;

fabricating a plurality of semiconductor devices on each wafer of the semiconductor wafers;

electronically probing each semiconductor device of the semiconductor devices on each wafer of the plurality of wafers to identify good, bad and repairable semiconductor devices on each wafer of the plurality of wafers;

repairing the repairable semiconductor devices;

programming each semiconductor device of the semiconductor devices on each wafer of the plurality of wafers to store a unique fuse identification;

storing an electronic wafer map for each wafer that identifies the locations of good and bad semiconductor devices on the wafer and associates each semiconductor device on the wafer with its fuse identification;

storing data in association with the fuse identification of each semiconductor device of the semiconductor devices identifying repairs performed on each semiconductor device of the semiconductor devices;

mounting each wafer of the plurality of wafers on an adhesive film;

sawing each semiconductor device of the semiconductor devices on each wafer of the wafers from its wafer to form a semiconductor device;

accessing the stored wafer map for each wafer;

accessing the stored data for each semiconductor device of the semiconductor devices on each of the wafers;

automatically picking each semiconductor device of the good semiconductor devices from its wafer;

discarding non-picked semiconductor devices identified as bad by the accessed wafer maps;

diverting picked semiconductor devices identified as good but unrepairable by the accessed wafer maps and data to a non-MCM device manufacturing process;

flip-chip attaching picked semiconductor devices identified as good and repairable by the accessed wafer maps and data to bonding sites of each printed circuit board of a plurality of printed circuit boards to form a plurality of MCM's;

curing each MCM of the plurality of MCM's;

testing each semiconductor device of the semiconductor devices on each MCM of the plurality of MCM's for opens and shorts;

encapsulating each semiconductor device of the semiconductor devices on each MCM of the plurality of MCM's;

retesting each semiconductor device of the semiconductor devices on each MCM of the plurality of MCM's for opens and shorts;

burn-in testing each semiconductor device of the semiconductor devices on each MCM of the plurality MCM's;

back-end testing each semiconductor device of the semiconductor devices on each MCM of the plurality of MCM's;

automatically reading the fuse identification code of each semiconductor device of the semiconductor devices in each MCM of the plurality of MCM's;

accessing the data stored in association with the fuse identification code of each semiconductor device of the semiconductor devices;

for any semiconductor device of the semiconductor devices failing any one of the opens/shorts, burn-in, and back-end tests, evaluating the accessed data to determine whether the failing semiconductor devices may be repaired;

repairing any semiconductor device of the semiconductor devices determined in accordance with the accessed data to be repairable and returning the repaired MCM to the manufacturing process; and

replacing any semiconductor device of the semiconductor devices determined in accordance with the accessed data to be unrepairable with Known Good Die (KGD) die and returning the repaired MCM to the manufacturing process.

36. The method of claim 35, wherein the step of mounting the wafers comprises mounting each wafer of the plurality of wafers on an Ultraviolet (U.V.) adhesive film, wherein the method further comprises exposing the U.V. adhesive film to U.V. light to loosen the wafer from the film prior to picking and flip-chip attaching the semiconductor device.

37. The method of claim 35, further comprising singulating the printed circuit boards associated with each MCM of the plurality of MCM's.

38. A method in an integrated circuit semiconductor device in a Multi-Chip Module (MCM) manufacturing process for diverting good but unrepairable semiconductor devices from the process, the semiconductor devices being of the type to have a substantially unique identification code, the method comprising:

storing data in association with the identification code of each semiconductor device of the semiconductor devices identifying semiconductor devices that are good and repairable, that are good but unrepairable, and that are bad;

automatically reading the identification code of each semiconductor device of the semiconductor devices;

accessing the data stored in association with the identification code of each semiconductor device of the semiconductor devices;

diverting semiconductor devices identified as good but unrepairable by the accessed data to other semiconductor device manufacturing processes; and

discarding semiconductor devices identified as bad by the accessed data.

39. The method of claim 38, further comprising:

assembling at least one semiconductor device identified as good and repairable into at least one MCM.

40. A semiconductor device manufacturing process using data related to manufacturing procedures used previously that a plurality of integrated circuits of semiconductor devices have undergone for selecting manufacturing procedures a plurality of integrated circuits of a semiconductor devices are to undergo during manufacture, each semiconductor device having integrated circuits and having a substantially unique identification code, the manufacturing process comprising:

storing data in association with the identification code of each semiconductor device identifying manufacturing procedures the semiconductor device has undergone;

automatically reading the identification code of each semiconductor device; and

accessing the data stored in association with the identification code of each semiconductor device.

41. The process of claim 40, further comprising:

selecting manufacturing procedures each semiconductor device undergoes in accordance with the accessed data.

42. The process of claim 40, wherein the step of storing data comprises storing data that identifies repairs performed semiconductor device.

43. The process of claim 42, wherein the semiconductor device comprises Dynamic Random Access Memory (DRAM) semiconductor device, wherein storing data

comprises storing data that identifies spare rows and columns used in repairing the DRAM semiconductor device.

44. The process of claim 42, wherein the semiconductor device comprises Dynamic Random Access Memory (DRAM) semiconductor device, wherein storing data comprises storing data that identifies spare rows and columns available to effect repairs in the DRAM semiconductor device.

45. The process of claim 40, wherein the step of storing data comprises storing data at probe.

46. The process of claim 40, wherein the step of automatically reading the identification code of each semiconductor device comprises electrically retrieving a unique fuse ID programmed into each semiconductor device.

47. The process of claim 40, wherein the step of automatically reading the identification code of each semiconductor device comprises an identification code including one of fuse ID, dot code, and bar code.

48. The process of claim 40, wherein the step of automatically reading the identification code of each semiconductor device comprises a dot code.

49. The process of claim 40, wherein the step of automatically reading the identification code of each semiconductor device comprises an identification code including a bar code.

50. The process of claim 40, wherein the step of automatically reading the identification code of each semiconductor device comprises optically reading a unique ID code provided on each semiconductor device.

51. The process of claim 50, wherein the step of optically reading a unique identification code provided on each semiconductor device comprises optically reading a unique laser fuse ID programmed into each semiconductor device.

52. The process of claim 40, wherein the step of automatically reading the identification code of each semiconductor device comprises automatically reading the identification code of each semiconductor device at one of an opens/shorts test, a burn-in test, and a back-end test in the semiconductor device manufacturing process.

53. The process of claim 40, wherein the step of accessing the data stored in association with the identification code of each semiconductor device comprises accessing the data stored in association with the identification code of each semiconductor device at one of an opens/shorts test, a burn-in test, and a back-end test in the semiconductor device manufacturing process.

54. The process of claim 41, wherein selecting manufacturing procedures the semiconductor device undergoes in accordance with the accessed data comprises selecting repairs the semiconductor device undergoes in accordance with the accessed data.

55. The process of claim 54, wherein the semiconductor device comprises Dynamic Random Access Memory (DRAM) semiconductor device, wherein selecting repairs the semiconductor device undergoes comprises selecting spare rows and columns used to repair the DRAM semiconductor device.

56. The process of claim 41, wherein the step of selecting manufacturing procedures the semiconductor device undergoes in accordance with the accessed data comprises selecting whether the semiconductor device undergoes repair procedures.

57. The process of claim 56, wherein the semiconductor device comprise Dynamic Random Access Memory (DRAM) semiconductor device, wherein selecting whether the semiconductor device undergoes repair procedures comprises selecting whether the DRAM semiconductor device will be repaired in accordance with whether the accessed data indicates enough spare rows and columns are available in the semiconductor device to effect repairs.

58. The process of claim 41, wherein the step of selecting manufacturing procedures the semiconductor device will undergo in accordance with the accessed data comprises determining whether the semiconductor device will be assembled into Multi-Chip Modules (MCM's) in accordance with whether the accessed data indicates the semiconductor device is repairable.

59. The process of claim 40, further comprising assembling the semiconductor device into a packaged semiconductor device after the step of storing data and before the step of automatically reading the identification code of each semiconductor device.

60. A method of manufacturing semiconductor devices from wafers, the method comprising:

providing a plurality of wafers;

fabricating a plurality of semiconductor devices on at least one wafer of the plurality of wafers;

causing each semiconductor device on the at least one wafer to store a substantially unique identification code;

storing data in association with the identification code of each semiconductor device that identifies manufacturing procedures the semiconductor device has undergone;

separating each semiconductor device on the at least one wafer from its wafer to form at least one semiconductor device;

assembling the at least one semiconductor device into a semiconductor device assembly;

automatically reading the identification code associated with the at least one semiconductor device; and

accessing the data stored in association with the identification code associated with the at least one semiconductor device.

61. The method of claim 60, further comprising:

selecting manufacturing procedures the at least one semiconductor device undergoes in accordance with the accessed data.

62. The method of claim 60, wherein the step of fabricating a plurality of semiconductor devices on at least one wafer comprises fabricating semiconductor devices selected from a group comprising Dynamic Random Access Memory (DRAM) semiconductor device, Static Random Access Memory (SRAM) semiconductor devices, Synchronous DRAM (SDRAM) semiconductor devices, and processor semiconductor devices, Rambus in-line memory module type semiconductor devices, small outline Rambus in-line memory module type semiconductor devices, and personal computer memory format type semiconductor devices .

63. The method of claim 60, wherein the step of causing the semiconductor devices to store a substantially unique identification code comprises programming each semiconductor device on each of the wafers to permanently store a unique fuse ID.

64. The method of claim 60, wherein the step of causing the semiconductor devices to store a substantially unique identification code comprises applying a dot code to the semiconductor devices.

65. The method of claim 60, wherein the step of causing the semiconductor devices to store a substantially unique identification code comprises applying a bar code to the semiconductor devices.

66. The method of claim 60, wherein the step of programming each semiconductor device on each of the wafers to permanently store a unique fuse identification code comprises programming at least one of fuses and anti-fuses in each semiconductor device on each of the wafers to permanently store a unique fuse identification.

67. The method of claim 60, wherein the step of assembling each semiconductor device of the semiconductor dice into a semiconductor device assembly comprises:

picking each semiconductor device from its wafer;

placing each semiconductor device onto an epoxy coated bonding site of one lead frame of a plurality of lead frames;

curing the epoxy on the bonding site of each lead frame of the lead frames;

wire bonding each semiconductor device to its associated lead frame;

encapsulating each semiconductor device and its associated lead frame to form one of a plurality of semiconductor device assembly packages, each package having projecting leads;

curing each of the semiconductor device assembly packages;

de-flashing the projecting leads of each semiconductor device assembly package;

electroplating the projecting leads of each semiconductor device assembly package; and

singulating each semiconductor device assembly package into one semiconductor device assembly package of a plurality of discrete semiconductor device assembly packages.

68. The method of claim 60, wherein separating each semiconductor device on the at least one wafer from its wafer to form at least one semiconductor device wherein the step of assembling each semiconductor device of the semiconductor dice into a semiconductor device assembly comprises:

singulating at least one semiconductor device from the at least one wafer using a saw.

69. The method of claim 60, wherein separating each semiconductor device on the at least one wafer from its wafer to form at least one semiconductor device wherein the step of assembling each semiconductor device of the semiconductor dice into a semiconductor device assembly comprises:

singulating at least one semiconductor device from the at least one wafer using a laser.

70. The method of claim 60, wherein separating each semiconductor device on the at least one wafer from its wafer to form at least one semiconductor device wherein the step of assembling each semiconductor device of the semiconductor dice into a semiconductor device assembly comprises:

singulating at least one semiconductor device from the at least one wafer using a laser/water apparatus.

71. The method of claim 60, wherein separating each semiconductor device on the at least one wafer from its wafer to form at least one semiconductor device wherein the step of assembling each semiconductor device of the semiconductor dice into a semiconductor device assembly comprises:

singulating at least one semiconductor device from the at least one wafer using a cool laser apparatus.

72. The method of claim 60, wherein separating each semiconductor device on the at least one wafer from its wafer to form at least one semiconductor device wherein the step of assembling each semiconductor device of the semiconductor dice into a semiconductor device assembly comprises:

singulating at least one semiconductor device from the at least one wafer using a water jet apparatus.

73. The method of claim 60, wherein the step of assembling each semiconductor device into a semiconductor device assembly comprises assembling each semiconductor device into a semiconductor device assembly selected from a group comprising a wire bond/lead frame semiconductor device, a Chip-On-Board (COB) semiconductor device, a flip-chip semiconductor device, and a Board-Over-Chip (BOC) semiconductor device.

74. The method of claim 60, wherein the step of assembling each semiconductor device of the semiconductor dice into a semiconductor device assembly comprises:

mounting the at least one semiconductor device on one of a lead frame of a plurality of lead frames and a substrate;

encapsulating each semiconductor device and a portion of one of a lead frame and a substrate forming a semiconductor device assembly package; and

singulating the semiconductor device assembly package from one of a plurality of lead frames and a substrate to form one semiconductor device assembly package.

75. The method of claim 74, wherein the step of singulating the semiconductor device assembly package from one of a plurality of lead frames and a substrate to form one semiconductor device assembly package comprises the use of a saw.

76. The method of claim 74, wherein the step of singulating the semiconductor device assembly package from one of a plurality of lead frames and a substrate to form one semiconductor device assembly package comprises the use of a laser.

77. The method of claim 74, wherein the step of singulating the semiconductor

device assembly package from one of a plurality of lead frames and a substrate to form one semiconductor device assembly package comprises the use of a laser/water apparatus.

78. The method of claim 74, wherein the step of singulating the semiconductor device assembly package from one of a plurality of lead frames and a substrate to form one semiconductor device assembly package comprises the use of a cool laser.

79. The method of claim 74, wherein the step of singulating the semiconductor device assembly package from one of a plurality of lead frames and a substrate to form one semiconductor device assembly package comprises the use of a water jet.

80. A method of manufacturing semiconductor devices from a plurality of wafers, the method comprising:

providing a plurality of wafers;

fabricating a plurality of semiconductor devices on at least one wafer of the plurality of wafers;

causing at least one semiconductor device on the at least one wafer to store a substantially unique identification code;

storing data in association with the identification code of the at least one semiconductor device identifying manufacturing procedures the at least one semiconductor device has undergone;

separating the at least one semiconductor device and at least one other semiconductor device on the at least one wafer from its wafer to form at least two semiconductor devices on a portion of the at least one wafer;

assembling the at least two semiconductor devices into a semiconductor device assembly;

automatically reading the identification code associated with the at least two semiconductor devices; and

accessing the data stored in association with the identification code associated with the at least two semiconductor devices.

81. The method of claim 80, further comprising:

selecting manufacturing procedures the at least one semiconductor device undergoes in accordance with the accessed data.

82. The method of claim 80, wherein the step of fabricating a plurality of semiconductor devices on at least one wafer comprises fabricating semiconductor devices selected from a group comprising Dynamic Random Access Memory (DRAM) semiconductor device, Static Random Access Memory (SRAM) semiconductor devices, Synchronous DRAM (SDRAM) semiconductor devices, and processor semiconductor devices, Rambus in-line memory module type semiconductor devices, small outline Rambus in-line memory module type semiconductor devices, and personal computer memory format type semiconductor devices .

83. The method of claim 80, wherein the step of causing the at least one semiconductor device to store a substantially unique identification code comprises programming each semiconductor device on each of the wafers to permanently store a unique fuse ID.

84. The method of claim 80, wherein the step of causing the at least one semiconductor device to store a substantially unique identification code comprises applying a dot code to the semiconductor devices.

85. The method of claim 80, wherein the step of causing the at least one semiconductor device to store a substantially unique identification code comprises applying a bar code to the semiconductor devices.

86. The method of claim 83, wherein the step of programming each semiconductor device on each of the wafers to permanently store a unique fuse identification code comprises programming at least one of fuses and anti-fuses in each semiconductor device on each of the wafers to permanently store a unique fuse identification.

87. The method of claim 80, wherein the step of assembling the at least two semiconductor devices into a semiconductor device assembly comprises:
picking the at least two semiconductor devices from the wafer;
placing the at least two semiconductor devices onto a bonding site of a substrate;
encapsulating at least one semiconductor device of the at least two semiconductor devices to form one of at least one semiconductor device assembly package; and
singulating the at least one semiconductor device assembly package.

88. The method of claim 80, wherein separating the at least one semiconductor device and at least one other semiconductor device on the at least one wafer from its wafer to form at least two semiconductor devices on a portion of the at least one wafer comprises:
singulating the at least two semiconductor devices from the at least one wafer using a saw.

89. The method of claim 80, wherein separating the at least one semiconductor device and at least one other semiconductor device on the at least one wafer from its wafer to form at least two semiconductor devices on a portion of the at least one wafer comprises:
singulating the at least two semiconductor devices from the at least one wafer using a laser.

90. The method of claim 80, wherein separating the at least one semiconductor device and at least one other semiconductor device on the at least one wafer from its wafer to form at least two semiconductor devices on a portion of the at least one wafer comprises:

singulating the at least two semiconductor devices from the at least one wafer using a laser/water apparatus.

91. The method of claim 80, wherein separating the at least one semiconductor device and at least one other semiconductor device on the at least one wafer from its wafer to form at least two semiconductor devices on a portion of the at least one wafer comprises:

singulating the at least two semiconductor devices from the at least one wafer using a cool laser apparatus.

92. The method of claim 80, wherein separating the at least one semiconductor device and at least one other semiconductor device on the at least one wafer from its wafer to form at least two semiconductor devices on a portion of the at least one wafer comprises:

singulating the at least two semiconductor devices from the at least one wafer using a water jet apparatus.

93. The method of claim 80, wherein the step of assembling each semiconductor device into a semiconductor device assembly comprises assembling each semiconductor device into a semiconductor device assembly selected from a group comprising a wire bond/lead frame semiconductor device, a Chip-On-Board (COB) semiconductor device, a flip-chip semiconductor device, and a Board-Over-Chip (BOC) semiconductor device.

94. The method of claim 80, wherein the step of assembling the at least two semiconductor devices into a semiconductor device assembly comprises:

mounting the at least two semiconductor devices on a substrate;

encapsulating each semiconductor device and a portion of the substrate forming semiconductor device assembly packages; and

singulating the semiconductor device assembly packages.

95. The method of claim 94, wherein the step of singulating the semiconductor device assembly package from one of a plurality of lead frames and a substrate to form one semiconductor device assembly package comprises the use of a saw.

96. The method of claim 94, wherein the step of singulating the semiconductor device assembly package from one of a plurality of lead frames and a substrate to form one semiconductor device assembly package comprises the use of a laser.

97. The method of claim 94, wherein the step of singulating the semiconductor device assembly package from one of a plurality of lead frames and a substrate to form one semiconductor device assembly package comprises the use of a laser/water apparatus.

98. The method of claim 94, wherein the step of singulating the semiconductor device assembly package from one of a plurality of lead frames and a substrate to form one semiconductor device assembly package comprises the use of a cool laser.

99. The method of claim 94, wherein the step of singulating the semiconductor device assembly package from one of a plurality of lead frames and a substrate to form one semiconductor device assembly package comprises the use of a water jet.

100. A method of manufacturing semiconductor devices from a plurality of wafers, the method comprising:

providing a plurality of wafers;

fabricating a plurality of semiconductor devices on at least one wafer of the plurality of wafers;

causing at least one semiconductor device on the at least one wafer to store a substantially unique identification code;

storing data in association with the identification code of the at least one semiconductor device identifying manufacturing procedures the at least one semiconductor device has undergone;

assembling the at least one wafer into a semiconductor device assembly;

automatically reading the identification code associated with the at least one semiconductor device; and

accessing the data stored in association with the identification code associated with the at least one semiconductor device.

101. The method of claim 100, further comprising:

selecting manufacturing procedures the at least one semiconductor device undergoes in accordance with the accessed data.

102. The method of claim 100, wherein the step of fabricating a plurality of semiconductor devices on at least one wafer comprises fabricating semiconductor devices selected from a group comprising Dynamic Random Access Memory (DRAM) semiconductor device, Static Random Access Memory (SRAM) semiconductor devices, Synchronous DRAM (SDRAM) semiconductor devices, and processor semiconductor devices, Rambus in-line memory module type semiconductor devices, small outline Rambus in-line memory module type semiconductor devices, and personal computer memory format type semiconductor devices .

103. The method of claim 100, wherein the step of causing the at least one semiconductor device to store a substantially unique identification code comprises programming each semiconductor device on each of the wafers to permanently store a unique fuse ID.

104. The method of claim 100, wherein the step of causing the at least one semiconductor device to store a substantially unique identification code comprises applying a dot code to the semiconductor devices.

105. The method of claim 100, wherein the step of causing the at least one semiconductor device to store a substantially unique identification code comprises applying a bar code to the semiconductor devices.

106. The method of claim 103, wherein the step of programming at least one semiconductor device on the wafer to permanently store a unique fuse identification code comprises programming at least one of fuses and anti-fuses in the at least one semiconductor device on the wafer to permanently store a unique fuse identification.

107. The method of claim 100, wherein the step of assembling the at least one wafer into a semiconductor device assembly comprises assembling the wafer into a semiconductor device assembly selected from a group comprising a Chip-On-Board (COB) semiconductor device, a flip-chip semiconductor device, and a Board-Over-Chip (BOC) semiconductor device.

108. The method of claim 100, wherein the step of assembling the at least one wafer into a semiconductor device assembly comprises:

mounting the wafer on a substrate; and

encapsulating the wafer and a portion of the substrate forming a wafer scale semiconductor device assembly package.

ABSTRACT OF THE DISCLOSURE

An inventive method in an integrated circuit (IC) manufacturing process for using data regarding repair procedures conducted on IC's at probe to determine whether any further repairs will be conducted later in the manufacturing process includes storing the data in association with a fuse ID of each of the IC's. The ID codes of the IC's are automatically read, for example, at an opens/shorts test during the manufacturing process. The data stored in association with the ID codes of the IC's is then accessed, and additional repair procedures the IC's may undergo are selected in accordance with the accessed data. Thus, for example, the accessed data may indicate that an IC is unrepairable, so the IC can proceed directly to a scrap bin without having to be queried to determine whether it is repairable, as is necessary in traditional IC manufacturing processes.

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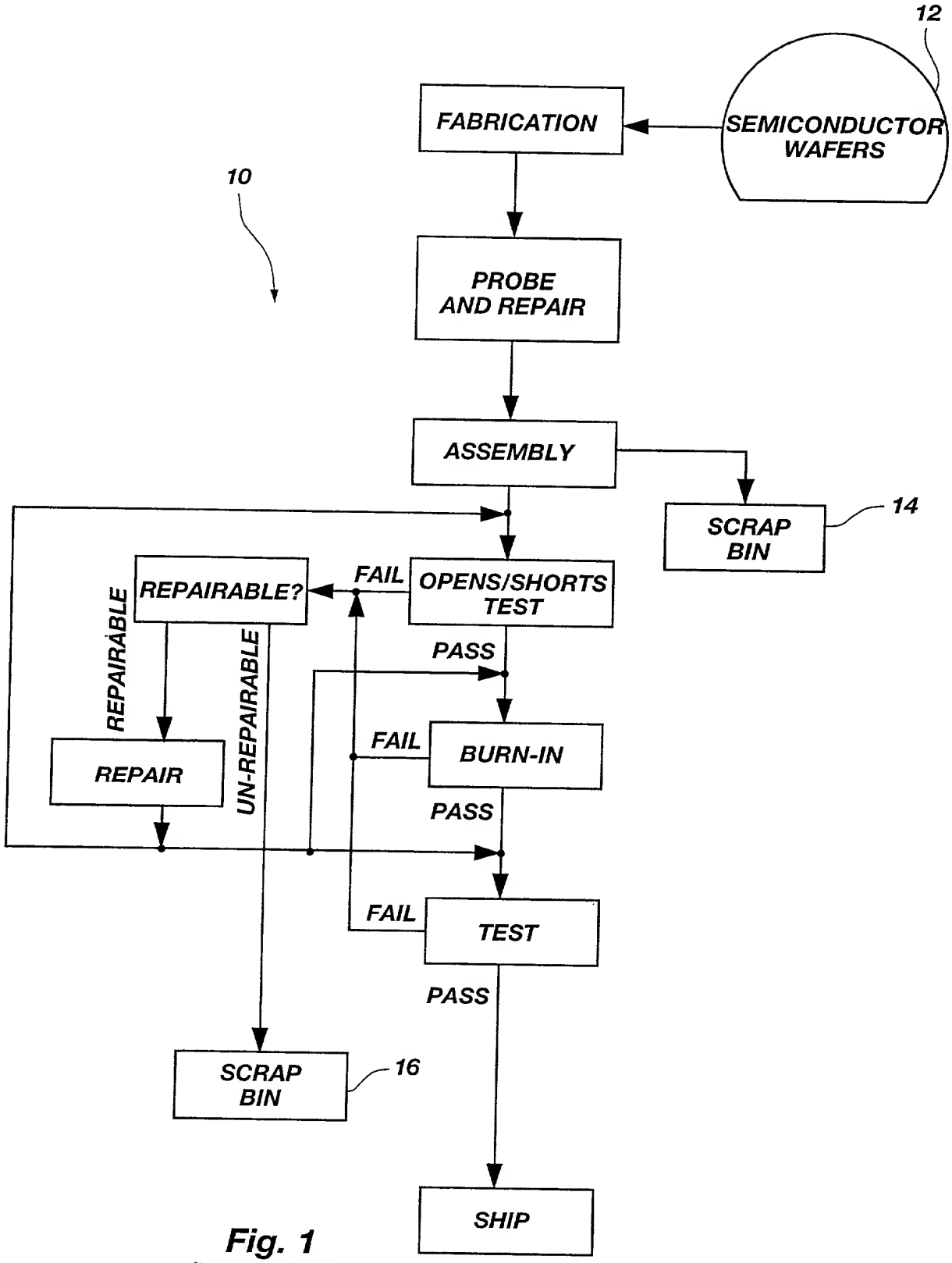


Fig. 1
(PRIOR ART)

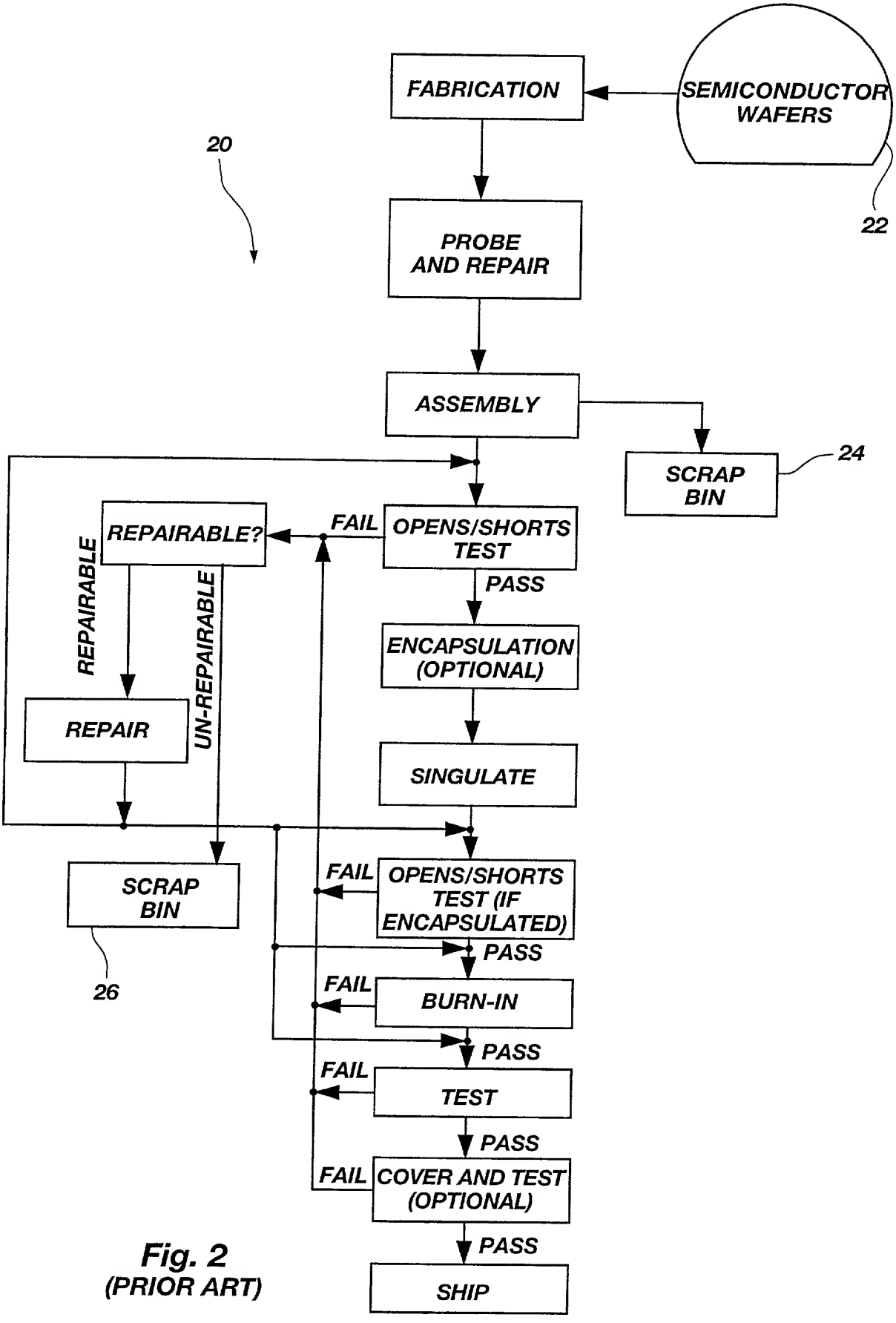


Fig. 2
(PRIOR ART)

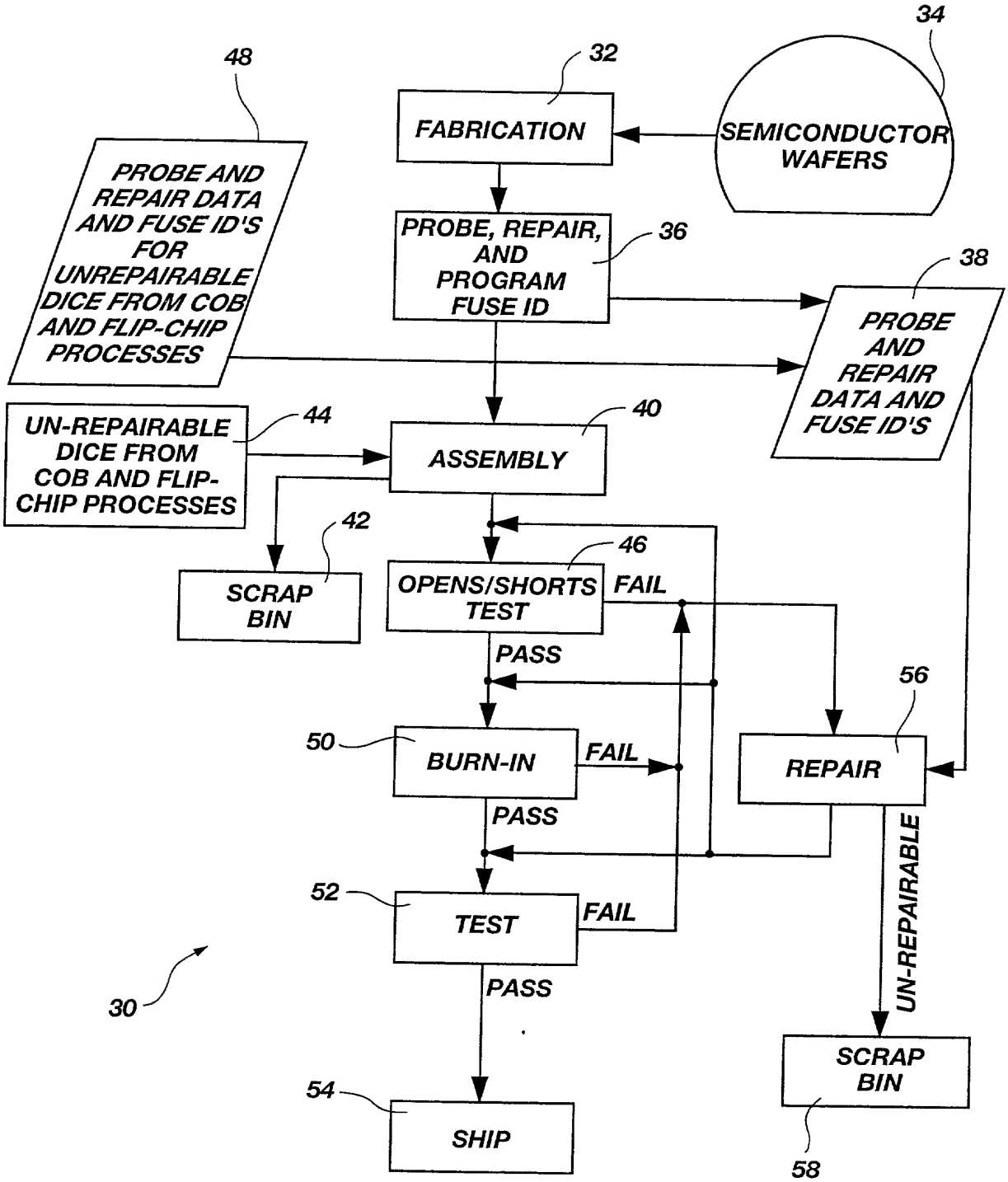
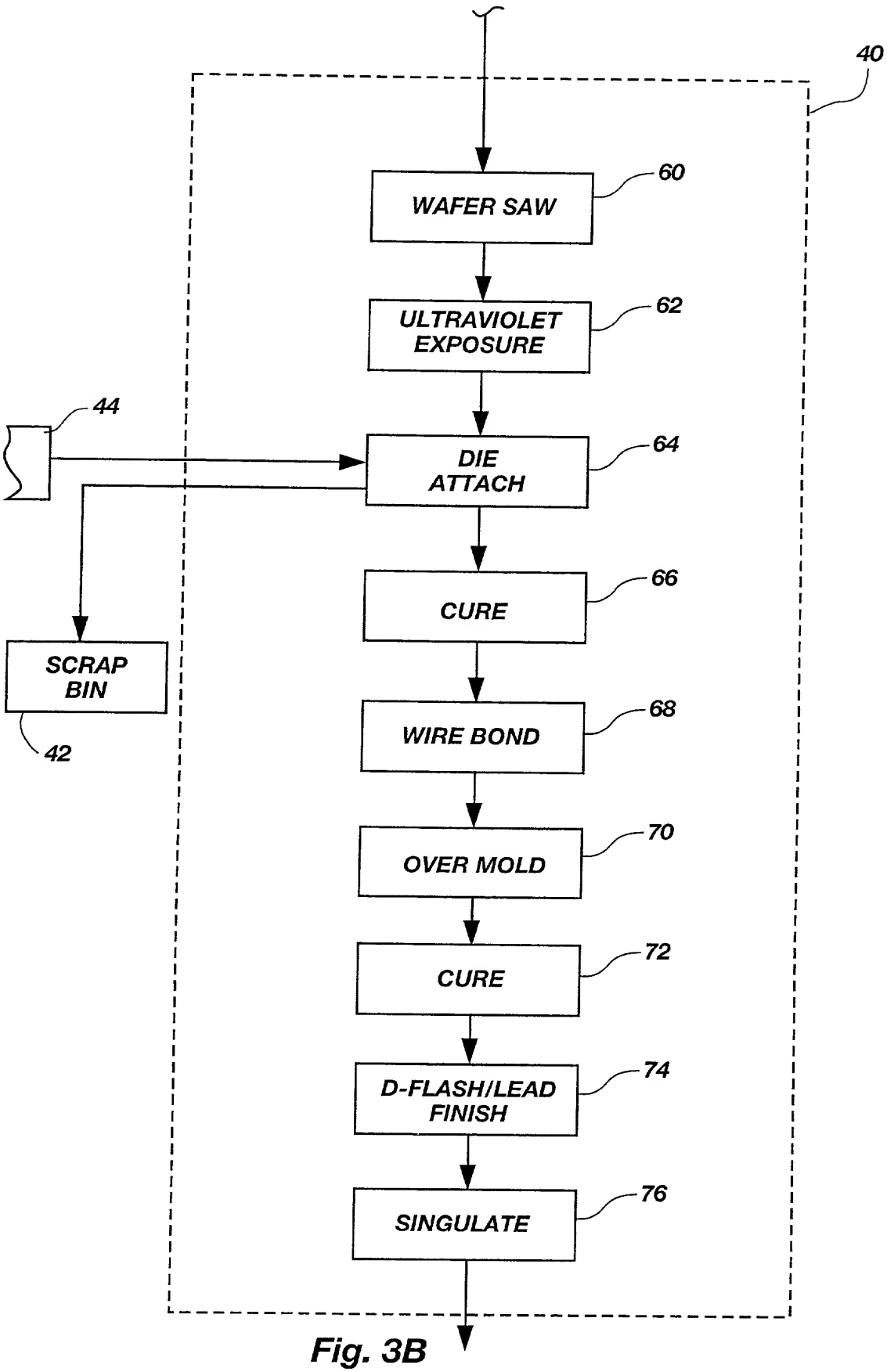

34
48
32
FABRICATION
SEMICONDUCTOR WAFERS
PROBE AND REPAIR DATA AND FUSE ID'S FOR UNREPAIRABLE DICE FROM COB AND FLIP-CHIP PROCESSES
PROBE, REPAIR, AND PROGRAM FUSE ID
36
38
PROBE AND REPAIR DATA AND FUSE ID'S
UN-REPAIRABLE DICE FROM COB AND FLIP-CHIP PROCESSES
44
40
ASSEMBLY
42
SCRAP BIN
46
OPENS/SHORTS TEST
FAIL
PASS
56
50
BURN-IN
FAIL
REPAIR
PASS
52
TEST
FAIL
UN-REPAIRABLE
30
PASS
SCRAP BIN
54
SHIP
58

Fig. 3A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WAFER SAW
60
ULTRAVIOLET EXPOSURE
62
44
DIE ATTACH
64
CURE
66
SCRAP BIN
42
WIRE BOND
68
OVER MOLD
70
CURE
72
D-FLASH/LEAD FINISH
74
SINGULATE
76

Fig. 3B

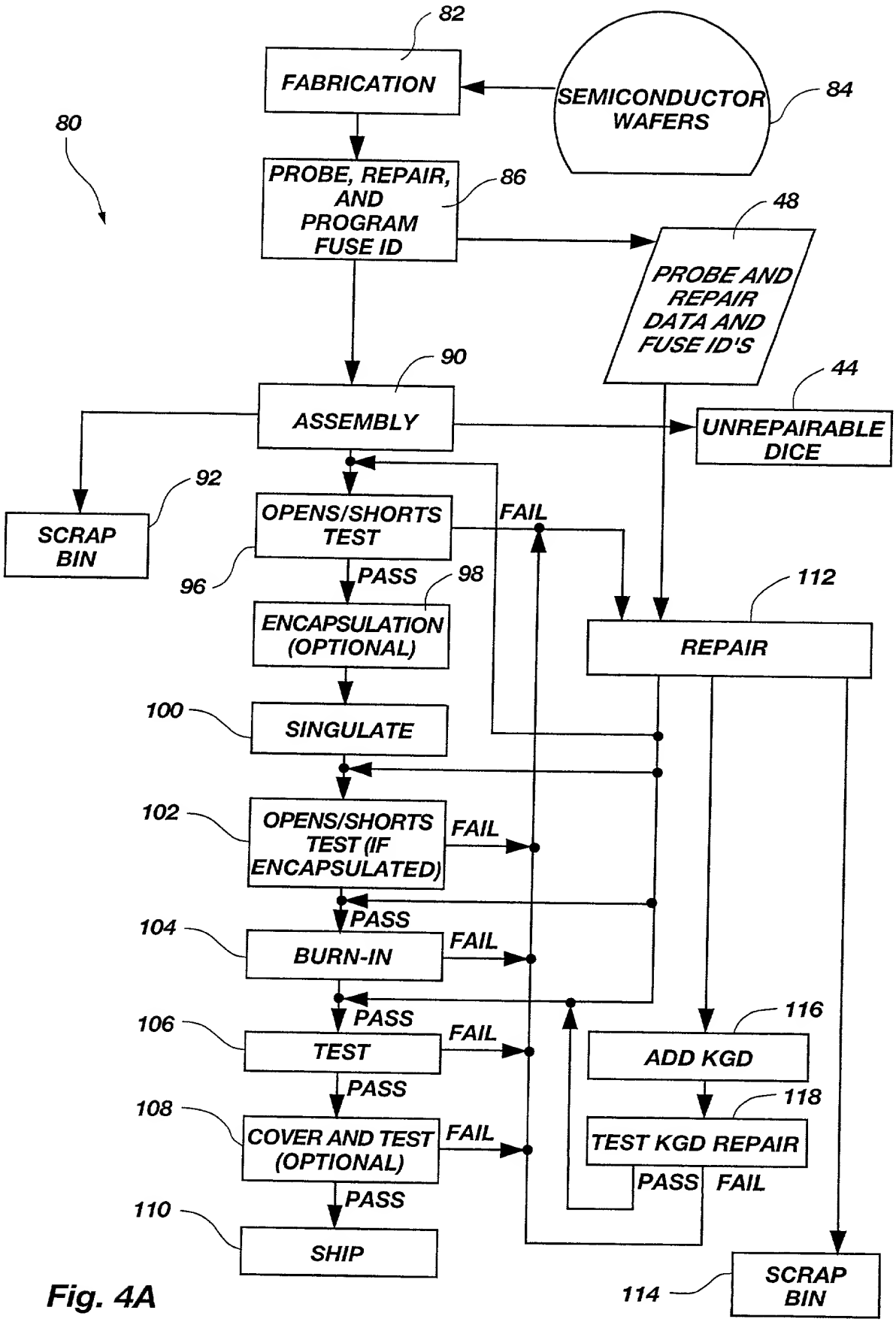
80
82
FABRICATION
SEMICONDUCTOR WAFERS
84
PROBE, REPAIR, AND PROGRAM FUSE ID
86
48
PROBE AND REPAIR DATA AND FUSE ID'S
90
ASSEMBLY
44
UNREPAIRABLE DICE
92
SCRAP BIN
OPENS/SHORTS TEST
FAIL
96
PASS
98
ENCAPSULATION (OPTIONAL)
112
REPAIR
100
SINGULATE
102
OPENS/SHORTS TEST (IF ENCAPSULATED)
FAIL
PASS
104
BURN-IN
FAIL
PASS
106
TEST
FAIL
116
ADD KGD
PASS
108
COVER AND TEST (OPTIONAL)
FAIL
118
TEST KGD REPAIR
PASS
FAIL
PASS
110
SHIP
114
SCRAP BIN

Fig. 4A

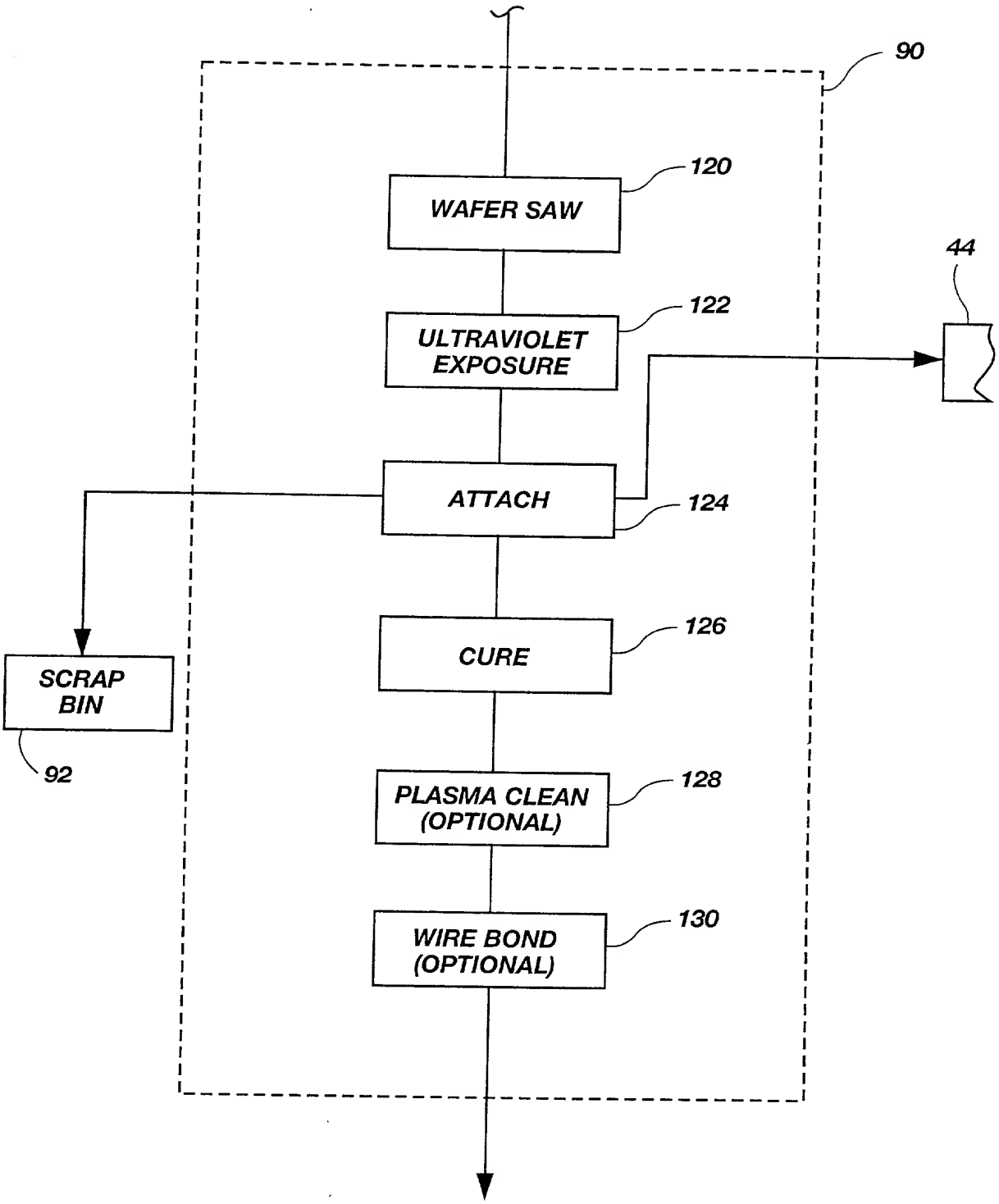
90
120
WAFER SAW
44
122
ULTRAVIOLET EXPOSURE
ATTACH
124
126
CURE
SCRAP BIN
92
128
PLASMA CLEAN (OPTIONAL)
130
WIRE BOND (OPTIONAL)

Fig. 4B

DECLARATION FOR PATENT APPLICATION (WITH POWER OF ATTORNEY)

As an inventor named below or on any attached continuation page, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name.

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled METHOD FOR USING DATA REGARDING MANUFACTURING PROCEDURES INTEGRATED CIRCUITS (IC'S) HAVE UNDERGONE, SUCH AS REPAIRS, TO SELECT PROCEDURES THE IC'S WILL UNDERGO, SUCH AS ADDITIONAL REPAIRS, the specification of which (check one):

- ☒ is attached hereto.
- ☐ was filed on _____ as United States application serial no. _____ and was amended on _____.
- ☐ was filed on _____ as PCT international application no. _____ and was amended under PCT Article 19 on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to the patentability of the subject matter claimed in this application, as "materiality" is defined in Title 37, Code of Federal Regulations § 1.56.

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or § 365(c) of PCT international application(s) designating the United States of America listed below and on any attached continuation page and, insofar as the subject matter of each of the claims of this application is not disclosed in any such prior application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations § 1.56 which became available between the filing date of such prior application and the national or PCT international filing date of this application:

Application Serial No.	Filing Date	Status
09/292,655	April 15, 1999	Pending
08/871,015	June 6, 1997	Patented
08/591,238	January 17, 1996	Pending
09/032,417	February 27, 1998	Pending
08/664,109	June 13, 1996	Pending
08/785,353	January 17, 1997	Pending
08/801,565	February 17, 1997	Patented
08/806,442	February 26, 1997	Pending
08/822,731	March 24, 1997	Pending

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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DECLARATION FOR PATENT APPLICATION
(continuation page)

Invention title: METHOD FOR USING DATA REGARDING MANUFACTURING PROCEDURES INTEGRATED CIRCUITS (IC'S) HAVE UNDERGONE, SUCH AS REPAIRS, TO SELECT PROCEDURES THE IC'S WILL UNDERGO, SUCH AS ADDITIONAL REPAIRS

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